**EXAMINER'S AMENDMENT**

1. An examiner's amendment to the record appears below. Should the changes and/or additions be unacceptable to applicant, an amendment may be filed as provided by 37 CFR 1.312. To ensure consideration of such an amendment, it MUST be submitted no later than the payment of the issue fee.

2. Authorization for this examiner's amendment was given in a telephone interview with Jon E. Holland (Reg No. 41,077) on 02/10/2009.

***In the Claims:***

Please amend the claims as follows:

1. (Currently Amended) A processor purging system, comprising:

a translation lookaside buffer (TLB) resident on a processor and having a plurality of translation pairs;

~~at least one memory cache~~ a component resident on the processor; and

logic configured to receive a purge signal and to make a determination whether ~~at least one~~ any of the translation pairs in the TLB corresponds to [[a]] the purge signal, the logic configured [[and]] to purge, in response to the purge signal, ~~each~~ one of the translation pairs in the TLB ~~corresponding~~ if any of the translation pairs in the TLB corresponds to the purge signal, the logic further configured to ~~transmit, based on the determination, a purge detection signal indicative of whether at least one~~

~~translation pair in the TLB corresponds to the purge signal and to determine, based upon the purge detection signal,~~ determine, based on whether any of the translation pairs in the TLB corresponds to the purge signal, whether to search the ~~memory cache~~ component resident on the processor for information ~~to be purged based on~~ related to ~~the purge signal~~ an address indicated by the purge signal, the logic further configured to purge the information from the component in response to the purge signal if any of the translation pairs in the TLB corresponds to the purge signal.

2. (Canceled)

3. (Currently Amended) The system of claim 1, wherein the ~~memory cache further~~ component comprises an instruction queue.

4. (Currently Amended) The system of claim 3, wherein the ~~memory cache further~~ component comprises a mini-TLB.

5. (Previously Presented) The system of claim 1, further wherein the logic is configured to compare the purge signal with each of the plurality of translation pairs and to transmit a plurality of match signals corresponding respectively to the plurality of translation pairs, each of the match signals indicating whether the corresponding translation pair corresponds to the purge signal.

6. (Currently Amended) The system of claim 5, wherein the logic is further configured to collapse the match signals into [[the]] a purge detection signal, and wherein the logic is configured to determine, based on the purge detection signal, whether to search the component for the information.

7. (Previously Presented) The system of claim 6, wherein the logic comprises a plurality of tiered logical AND gates configured to collapse the match signals into the purge detection signal.

8. (Previously Presented) The system of claim 6, wherein the logic comprises a plurality of tiered logical OR gates configured to collapse the match signals into the purge detection signal.

9-11. (Canceled)

12. (Currently Amended) A method for purging a processor, comprising ~~the steps of~~:

detecting whether ~~at least one~~ any of a plurality of translation pairs in a translation lookaside buffer (TLB) corresponds to a purge signal;

if ~~at least one of the~~ any of the translation pairs in the TLB corresponds to the purge signal, purging the ~~at least one~~ translation pair corresponding to the purge signal;

~~transmitting, based on the detecting step, a purge detection signal indicative of~~ determining whether to search an instruction queue for information related to an address indicated by the purge signal based on whether any of the ~~at least one of the~~ translation pairs in the TLB corresponds to the purge signal; and

~~determining whether to purge an~~ purging the information from the instruction queue based on the ~~purge detection signal~~ determining.

13. (Currently Amended) The method of claim 12, wherein the detecting ~~step~~ further comprises ~~the steps of~~:

comparing the purge signal with each of the translation pairs; and

transmitting match signals, each of the match signals indicative of whether a respective one of the translation pairs corresponds to the purge signal.

14. (Currently Amended) The method of claim 13, further comprising ~~the step of~~ collapsing each of the match signals into the purge detection signal.

15-16. (Canceled)

17. (Currently Amended) A processor purging method, comprising:

detecting whether ~~at least one~~ any of ~~translation pair in~~ a plurality of translation pairs within a translation lookaside buffer (TLB) resident on a processor corresponds to a purge signal;

~~transmitting, based on the detecting step, a purge detection signal indicative of whether at least one of the translation pairs corresponds to the purge signal;~~

determining, based upon the purge detection signal, whether to search ~~the memory cache~~ a component resident on the processor for information ~~to be purged based on~~ related to an address indicated by the purge signal based on whether any of the plurality of translation pairs within the TLB corresponds to the purge signal;

purging the information from the component in response to the determining; and

if ~~at least one~~ any of the translation pairs in the TLB corresponds to the purge signal, purging from the TLB the ~~at least one~~ translation pair corresponding to the purge signal.

18-22. (Canceled)

23. (Currently Amended) The method of claim 12, wherein the determining ~~step~~ comprises ~~the step of~~ determining not to ~~purge~~ search the instruction queue for the information in response to the purge signal if none of the translation pairs corresponds to the purge signal.

24. (Currently Amended) The method of claim 17, wherein the component comprises an instruction queue, and wherein the method further ~~comprising~~ comprises ~~the step of~~ purging [[an]] the instruction queue in response to the purge signal if a detection is made in the detecting step that ~~at least one~~ any of the translation pairs within the TLB corresponds to the purge signal.

25. (Currently Amended) A processor, comprising:

an execution unit;

an instruction queue coupled to the execution unit;

a translation lookaside buffer (TLB) configured to store a plurality of translation pairs, each

translation pair having a respective virtual address and a respective physical address; and

logic configured to receive a purge signal and to make a determination as to whether any of the translation pairs stored in the TLB corresponds to the purge signal, the logic configured to purge from the TLB ~~each~~ one of the translation pairs if any of the translation pairs stored in the TLB corresponds ~~corresponding~~ to the purge signal, the logic further configured to determine, based on the determination, whether to search the instruction queue for information related to an address indicated by the purge signal and to purge the information from the instruction queue ~~in response~~ if any of the translation pairs stored in the TLB corresponds to the purge signal.

26. (Canceled)

27. (Currently Amended) The processor of claim [[26]] 25, wherein the logic is configured to refrain from purging the instruction queue in response to the purge signal unless ~~at least one of the~~ a translation ~~pairs~~ pair stored in the TLB corresponds to the purge signal.

28. (Currently Amended) A method, comprising ~~the steps of~~:

storing a plurality of translation pairs in a translation lookaside buffer (TLB) resident on a processor, each of the translation pairs having a respective virtual address and a respective physical address;

receiving a purge signal identifying ~~at least one~~ a stale translation pair;

determining whether any of the plurality of translation pairs in the TLB [[are]] is identified by the purge signal;

if ~~at least one of the plurality of~~ a translation ~~pairs~~ pair in the TLB is identified by the purge signal, purging the ~~at least one~~ translation pair identified by the purge signal; and

determining whether to ~~purge at least one~~ purge, from a component ~~of a memory cache~~ resident on the processor other than the TLB, information related to an address indicated by the purge signal based on the ~~step of~~ determining whether any of the plurality of translation pairs in the TLB [[are]] is identified by the purge signal.

29. (Currently Amended) The method of claim 28, wherein the ~~step of~~ determining whether to purge ~~the at least one component step~~ comprises ~~the step of~~ determining not to purge the ~~at least one~~ component if none of the translation pairs in the TLB is identified by the purge signal.

30. (Currently Amended) The method of claim 28, further comprising ~~the step of~~, if ~~at least one of the plurality of~~ a translation ~~pairs~~ pair in the TLB is identified by the purge signal, purging the ~~at least one~~ component in response to the ~~step of~~ determining whether to purge ~~the at least one component~~.

31. (Currently Amended) The method of claim 30, wherein the ~~at least one~~ component comprises an instruction queue.

-- END OF AMENDMENT --

***Conclusion***

Any inquiry concerning this communication or earlier communications from the examiner should be directed to ERIC C. WAI whose telephone number is (571)270-1012. The examiner can normally be reached on Mon-Fri, 9am-5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Meng - Ai An can be reached on 571-272-3756. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

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